In the Claims

Claim 1 (cancelled).

Claim 2 (currently amended): ~~The method of claim 1 further comprising:~~ A method of forming a low electrical resistance metal silicide, comprising:

forming a first metal silicide layer over a substrate, the first metal silicide layer having a melting point higher than 1700°C and being metal-enriched, the first metal silicide layer having a thickness of at least about 50Å and comprising a predominate metal;

forming a metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being a metal different than the predominant metal of the first metal silicide;

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate; the second metal silicide layer having a bulk resistance of less than 30 micro-ohms-centimeter;

prior to converting the metal of the metal-containing layer to the second metal silicide layer, forming a silicon-containing layer directly against the metal-containing layer and on an opposing side of the metal-containing layer from the first metal silicide layer; and

wherein the conversion of the metal of the metal-containing layer to the second metal silicide layer comprises incorporation of silicon from the silicon-containing layer into the second metal silicide layer.

Claim 3 (original): The method of claim 2 wherein the first metal silicide layer is formed on a non-silicon-containing electrically conductive material.

Claim 4 (original): The method of claim 2 wherein the silicon-containing layer is formed to a thickness of at least about 400Å.

Claim 5 (original): The method of claim 2 further comprising incorporating the second metal silicide layer into a bitline.

Claims 6-13 (cancelled).

Claim 14 (currently amended): ~~The method of claim 1 further comprising~~ A method of forming a low electrical resistance metal silicide, comprising:

forming a first metal silicide layer over a substrate, the first metal silicide layer having a melting point higher than 1700°C and being metal-enriched, the first metal silicide layer having a thickness of at least about 50Å and comprising a predominate metal;

forming a metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being a metal different than the predominant metal of the first metal silicide;

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate; the second metal silicide layer having a bulk resistance of less than 30 micro-ohms-centimeter; and

prior to the converting, forming a layer consisting essentially of silicon or conductively-doped silicon directly against the metal-containing layer and on an opposing side of the metal-containing layer from the first metal silicide layer ~~prior to the converting~~.

Claim 15 (original): The method of claim 14 further comprising forming a silicon nitride cap over the layer consisting essentially of silicon or conductively-doped silicon during the converting.

Claim 16 (original): The method of claim 14 wherein the substrate comprises silicon, and wherein the first metal silicide layer is formed directly against the silicon of the substrate.

Claims 17-29 (cancelled).

Claim 30 (currently amended): ~~The method of claim 17 further comprising~~ A method of forming metal silicide comprising metal from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table, the method comprising:

forming a first metal silicide layer over a substrate, the metal of the first metal silicide layer predominately being a refractory metal, the first metal silicide layer having a thickness of at least about 50Å;

forming a metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table and being different than the predominate refractory metal of the first metal silicide layer;

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate; and

prior to the converting, forming a layer comprising silicon directly against the metal-containing layer and on an opposing side of the metal-containing layer from the first metal silicide layer ~~prior to the converting~~.

Claim 31 (currently amended): ~~The method of claim 17 further comprising~~ A method of forming metal silicide comprising metal from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table, the method comprising:

forming a first metal silicide layer over a substrate, the metal of the first metal silicide layer predominately being a refractory metal, the first metal silicide layer having a thickness of at least about 50Å;

forming a metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table and being different than the predominate refractory metal of the first metal silicide layer;

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate; and

prior to the converting, forming a layer consisting essentially of silicon or conductively-doped silicon directly against the metal-containing layer and on an opposing side of the metal-containing layer from the first metal silicide layer ~~prior to the converting~~.

Claim 32 (original): The method of claim 31 further comprising forming a silicon nitride cap over the layer consisting essentially of silicon or conductively-doped silicon during the converting.

Claim 33 (currently amended): The method of claim ~~17~~ 32 wherein the converting comprises exposing the metal-containing layer and the first metal silicide layer to a temperature of from about 600°C to about 900°C for a time of at least about 30 seconds.

Claim 34 (currently amended): The method of claim ~~17~~ 32 further comprising incorporating the second metal silicide layer into a wordline of an integrated circuit.

Claim 35 (original): The method of claim 34 wherein the wordline has a width of less than or equal to 0.25 micrometers.

Claim 36 (original): The method of claim 34 wherein the wordline has a width of less than or equal to 0.15 micrometers.

Claim 37 (original): The method of claim 34 wherein the wordline has a width of less than or equal to 0.11 micrometers.

Claim 38 (currently amended): The method of claim ~~17~~ 32 further comprising incorporating the second metal silicide layer into a bitline of an integrated circuit.

Claim 39 (original): The method of claim 38 wherein the bitline has a width of less than or equal to 0.25 micrometers.

Claim 40 (original): The method of claim 38 wherein the bitline has a width of less than or equal to 0.15 micrometers.

Claim 41 (original): The method of claim 38 wherein the bitline has a width of less than or equal to 0.11 micrometers.

Claims 42-47 (cancelled).

Claim 48 (currently amended): ~~The method of claim 42 further comprising~~ A method of forming titanium silicide, comprising:

forming a metal silicide layer over a substrate, the metal silicide layer consisting essentially of MSi_x where x is greater than 0 and where M is one or more metals other than titanium, the metal silicide layer having a thickness of at least about 50Å;

forming a titanium-containing layer directly against the metal silicide layer;

after forming the titanium-containing layer directly against the metal silicide layer, converting the titanium to titanium silicide; and

prior to the converting, forming a layer consisting essentially of silicon or conductively-doped silicon directly against the titanium-containing layer and on an opposing side of the titanium-containing layer from the metal silicide layer ~~prior to the converting~~.

Claim 49 (original): The method of claim 48 wherein the substrate comprises silicon, and wherein the metal silicide layer is formed directly against the silicon of the substrate.

Claim 50 (currently amended): The method of claim ~~42~~ 48 wherein the converting comprises exposing the titanium-containing layer and the metal silicide layer to a temperature of from about 600°C to about 900°C for a time of at least about 30 seconds.

Claim 51 (currently amended): The method of claim ~~42~~ 48 further comprising incorporating the titanium silicide into a wordline of an integrated circuit.

Claim 52 (original): The method of claim 51 wherein the wordline has a width of less than or equal to 0.25 micrometers.

Claim 53 (original): The method of claim 51 wherein the wordline has a width of less than or equal to 0.15 micrometers.

Claim 54 (original): The method of claim 51 wherein the wordline has a width of less than or equal to 0.11 micrometers.

Claim 55 (currently amended): The method of claim ~~42~~ 48 further comprising incorporating the titanium silicide into a bitline of an integrated circuit.

Claim 56 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.25 micrometers.

Claim 57 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.15 micrometers.

Claim 58 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.11 micrometers.

Claims 59-81 (cancelled).

Claim 56 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.25 micrometers.

Claim 57 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.15 micrometers.

Claim 58 (original): The method of claim 55 wherein the bitline has a width of less than or equal to 0.11 micrometers.

Claims 59-81 (cancelled).